

Substitute for form 1449A&B/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				Application Number / Confirmation Number	10/660,449 / 4907
<i>(Use as many sheets as necessary)</i>				Filing Date	09/11/2003
				First Named Inventor	Warren E. Cory
				Art Unit	2182
				Examiner Name	Tanh Q. Nguyen
Sheet	1	of	2	Attorney Docket Number	X-1214 US

<b>U.S. PATENT DOCUMENTS</b>					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code <i>(if known)</i>			
/T.N./		US-6,995,618	2/7/2006	Boecker	
		US-6,908,340	6/21/2005	Shafer	
		US-6,812,870	11/2/2004	Kryzak et al.	
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		US-7,187,709	3/6/2007	Menon et al.	
		US-7,009,426	8/29/2006	Cory et al. <b>already cited in PTO-892</b>	
<b>NON PATENT LITERATURE DOCUMENTS on 03/25/08</b>					
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T <sup>2</sup>

Examiner Signature	/Tanh Nguyen/ (08/30/2008)	Date Considered	08/30/2008
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<sup>1</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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/T.N./		10/659,803 filed 9/11/2003, BLACK, WILLIAM C., et al., Analog Front-End Having Built-In Equalization and Applications Thereof, Xilinx, Inc. 2100 Logic Drive, San Jose, California 95124			
		10/660,254 filed 9/11/2003, GROEN, ERIC D., et al., MGT/FPGA Clock Management System, Xilinx, Inc. 2100 Logic Drive, San Jose, California 95124			
↓		10/661,016 filed, 9/11/2003, GROEN, ERIC D., et al., Programmable Logic Device Including Programmable Multi-Gigabit Transceivers, Xilinx, Inc. 2100 Logic Drive, San Jose, California 95124			

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